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AREA-TIME EFFICIENT ARCHITECTURE FOR FAST FOURIER TRANSFORM USING DIFFERENT MULTIPLIER TECHNIQUE

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ABSTRACT:

It is a well known fact that the multiplier unit forms an integral part of processor design. Due to this, high speed multiplier architecture became the need of the day. In his paper a novel programmable FFT architecture for radix-2 DIT algorithm using array multiplier, sign multiplier & complex multiplier is proposed.
This parallel-pipelined architecture for the computation of real and complex valued FFT reduce the hardware complexity. The folding transformation is proposd for designing FFT architecture.
Upon comparison, the proposed algorithm based on unsigned, signed & complex multiplier is fast than previous algorithm. For all design four experiment were carried out on a Xilinx 6.2i Virtex-2p device family.

KEYWORDS: *FFT, Folding Technique, Single Path Delay Feedback (SDF), Serial in Serial out Shift Register, Maximum Combinational Path Delay (MCPD), Look Up table (LUT).*

1. INTRODUCTION

The Fourier Transform is an inevitable approach in signal processing [1], the Discrete Fourier Transform decomposes a set of values into different components of frequency. The Fast Fourier transform (FFT) is an appropriate technique to do manipulation of DFT. The algorithm of FFT was devised by Cooley and Tukey in order to decrease the amount of complexity with respect to time and computations [2].

The hardware of FFT can be implemented by two types of classifications- memory architecture and pipeline architecture. The memory architecture, includes a solitary handling component and different units of memory [3]. The benefits of memory design incorporate low power and minimal effort when contrasted with that of different styles. The particular bad marks are more noteworthy inertness and lower throughput. The above negative marks of the memory design are completely dispensed with by pipeline engineering to the detriment of additional equipment in a worthy way. The different kinds of pipeline engineering incorporate Single postpone criticism (SDF), Single defer commutator (SDC) and various postpone commutator (MDC). The pipeline engineering is a normal structure which can be received by utilizing equipment portrayal dialect in a simple way.

The calculations of FFT can be assembled into settled radix, blended radix and split radix calculations in an unpleasant way [5]. The essential classes of calculations of FFT incorporate - Decimation in-recurrence (DIF) and the Decimation-in-time (DIT) as appeared in Figure 1. Both of these calculations rely upon deterioration of change of a N-point grouping into numerous subsequences in a progressive way. There is no real contrast between them to the extent multifaceted nature of calculation is concerned. By and large DIT manages the information and yield backward grouping and typical arrangement individually, while DIF manages information and yield in ordinary succession

and turn around succession separately. Just Decimation-in-Time (DIT) calculation is contemplated. In this paper for execution and result examination, anyway DIT calculation can likewise be utilize the proposed technique.

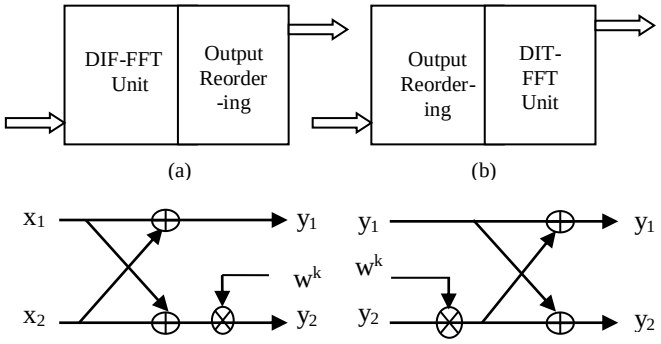

Fig. 1 (A) DIF FFT Processing (B) DIT FFT Processing (C) DIF FFT Butterfly (D) DIT FFT

The Input Sequence X(N) Of Size 'N' Is Decomposed Into Samples Of Odd And Even And The Corresponding Sub-Sequences $F_1(N)$ And $F_2(N)$ Are Given By:

$$f_1(n) = x(2n) \quad (1)$$

$$f_1(n) = x(2n+1),\ n = 0,1.....\frac{N}{2} - 1 \quad (2)$$

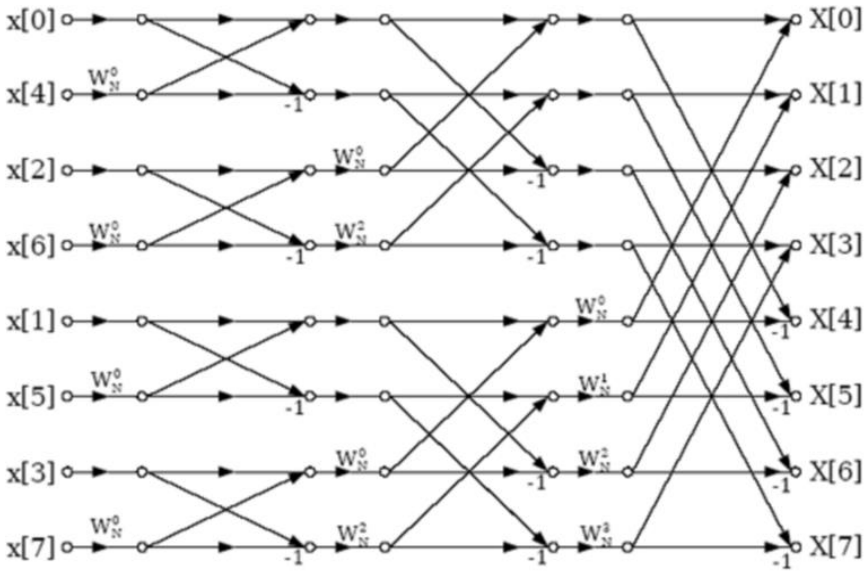

Fig. 2 Butterfly of Radix-2 DIT FFT Algorithm

In figure 2, show the butterfly of radix-2 DIT FFT algorithm. In this figure we used eight inputs and eight outputs. In case of DIT the input sample is used bit reversal order while the output of DIT FFT coefficients is generated in natural order. In Figure 2, show the butterfly of radix-2 DIT FFT algorithm. In case of DIT the input sample is used in natural order while the output of DIT FFT coefficient is generated in bit reversed order.

2. PROPOSED METHODOLOGY

In proposed method we are using serial input serial output (SISO) shift register as shown in Figure 3. In which binary input is required.Proposing algorithm consist of SISO shift register, different types of multiplier, adder, subtractor, single path delay feedback (SPD) pipeline and folding architecture as shown in figure 4 flow chart of algorithm.

2.1 SISO

serial in serial out (SISO) shift register are kind of shift register where both data loading as well as data retrivel to/from the shift register occurs in serial mode. Assume the twofold contribution of the framework is 8 word length, at that point eight postpone flip lemon are utilized in SISO enroll.

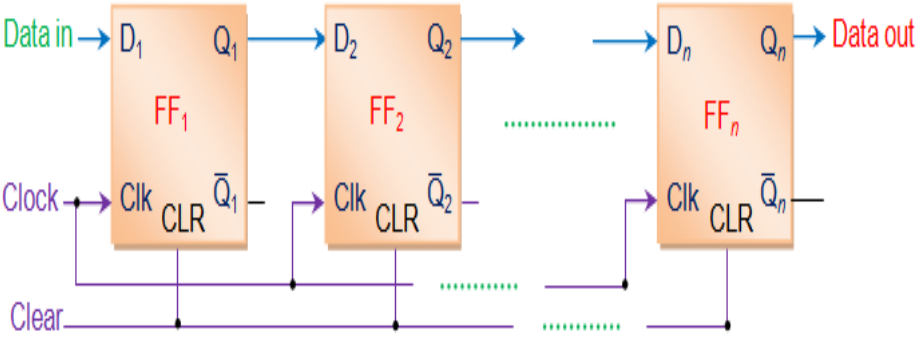

Fig.3 N-Bit Right-Shift Serial In Serial Out Shift Register

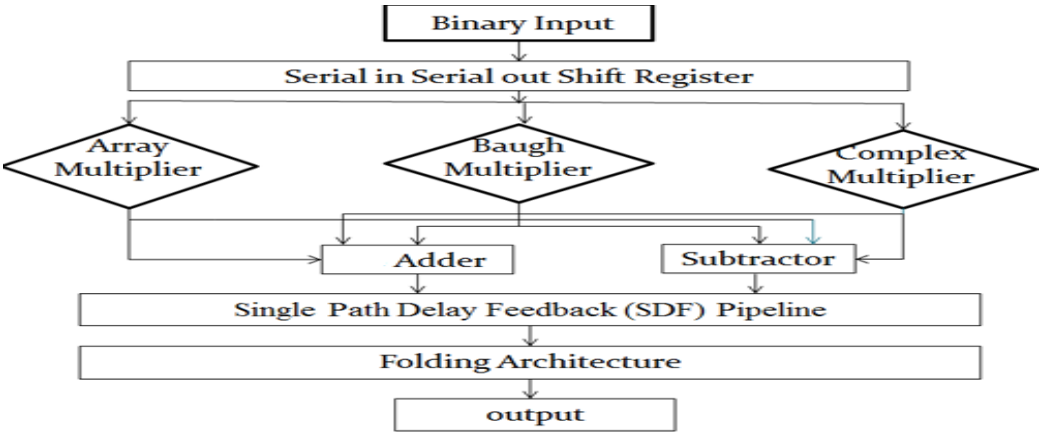

Fig. 4 Flow Chart of Proposed Algorithm

2.2 Different types of Multiplier

There are three types of multiplier are used in proposed algorithm, i.e. Array multiplier, sign (Baugh) multiplier and complex multiplier. Another name of array multiplier is binary unsigned multiplied.

The Baugh & Wooley algorithm for the signed binary multiplication is based on the concept shown in figure 5. The algorithm specifies that all possible AND terms are created white cell and all possible NAND terms are created gray cell. The white cell consists of full adder and AND gate, but the gray cell consists of full adder and NAND gate.

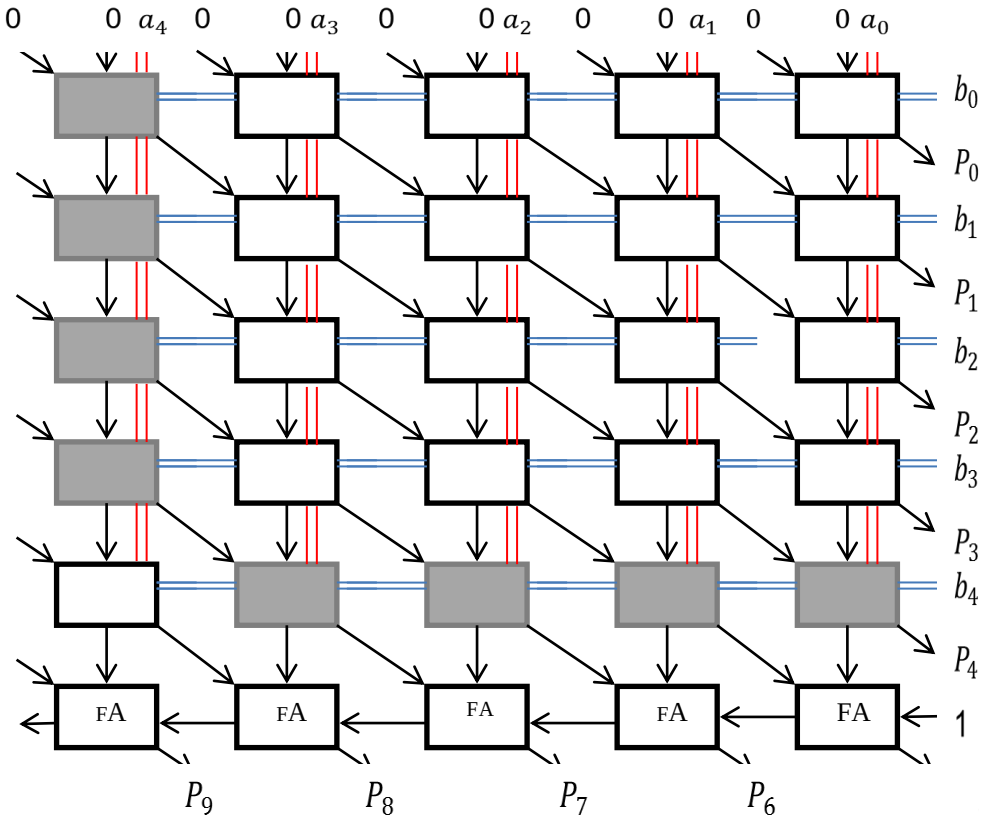

Fig. 5 Block Diagram of Sign Multiplier (Baugh &

Complex multiplication is consisting of 4 multiplications, 2 adders and 1 subtraction. But in the proposed complex multiplication is consisting of 3 multiplications, 1 adder and 1 subtraction in shown in figure 5.

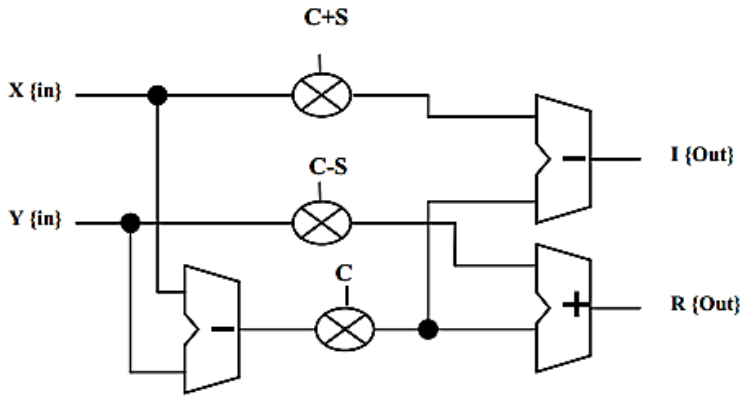

Fig. 6 Block Diagram of Complex Multiplication

2.3 Subtractor

subtractor is consist of half subtractor and full subtractor depends on word length in proposed algorithm.

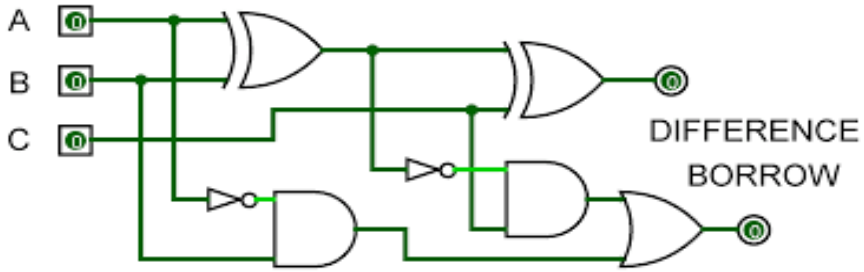

Fig. 7 Full Substractor Using Two Half Substractor

2.4 Adder

Information arrangement of conventional strategy is significantly more than to proposed technique, anyway proposed technique has less spread deferral. Territory and engendering postponement can be decreased by the guide of proposed snake. This snake will be structured like as swell convey adder.

2.5 Single

path delay feedback pipeline architecture:- herbert l. Groginsky and george a. Works introduced a feedback mechanism in order to minimize the number of delay elements. In the proposed architecture one half of outputs from each stage are feedback to the input data buffer when the input data are directly sent to the butterfly.

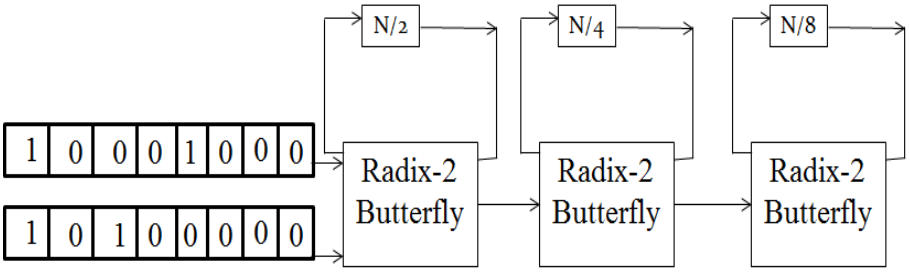

Fig.8 Flow Graph of the Radix-2 SDF Pipeline Architecture

2.6 Folding Architecture

Folding is a transformation technique using in DSP architecture, implementation for minimizing the number of functional blocks in synthesizing DSP architecture. Folding was first developed by Keshab K. Parhi and his students in 1992.

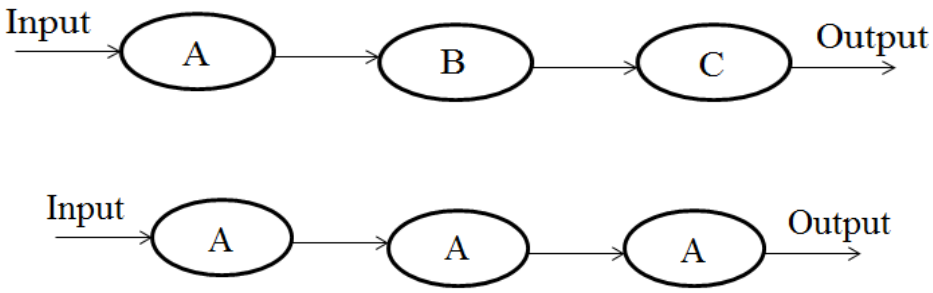

Fig. 9 (a) Without folding technique (b) With folding technique

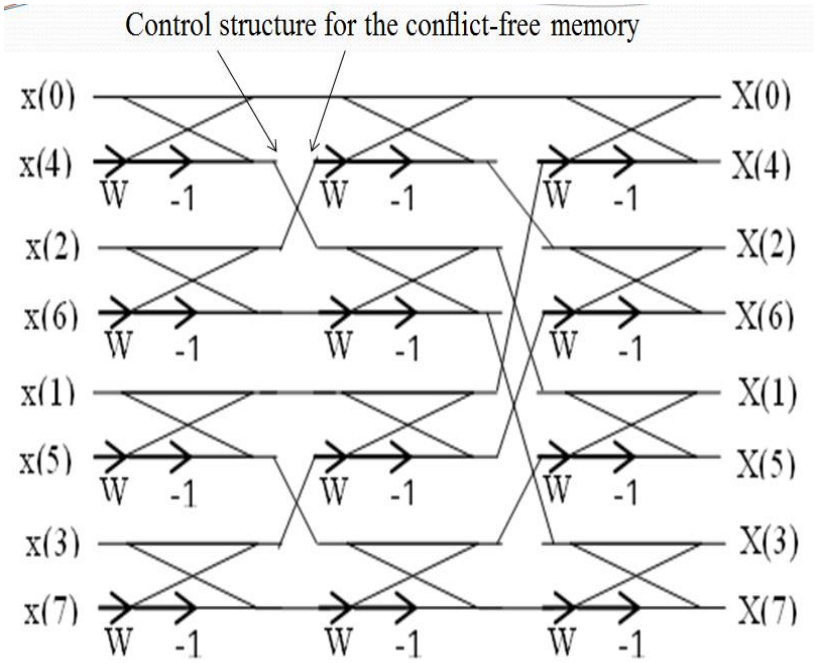

Fig. 10 Proposed DIT Radix-2 FFT algorithm using Radix-2 Butterfly

3. SIMULATION RESULT

The simulation results for various FFT algorithms have been tested practically by implementing in the Vertex-2p Xilinx software. Also these software outputs can be verified with simulation results obtained using MODELSIM. Some of the snapshots of results in the Xilinx software and simulation are as follows.

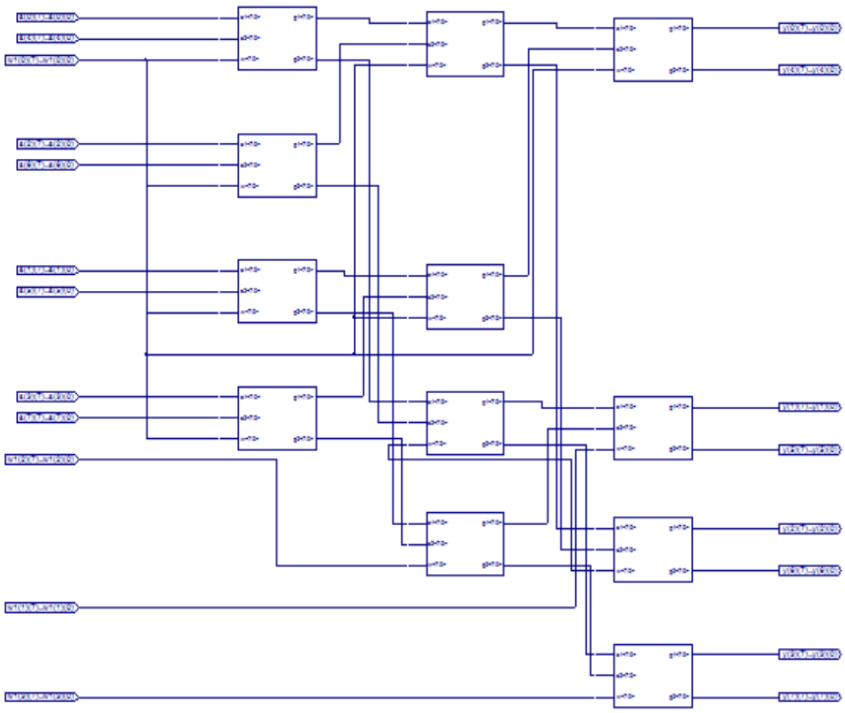

Fig. 11 RTL view of proposed DIT Radix-2 FFT algorithm

Table I. Show the result for proposed algorithm in array multiplier with Vertex-2p device family

Design	N	Number of slices	Number of 4 input LUTs	MCPD (nsec)
Proposed structure	8	97	192	15.598
	16	260	512	19.260
	32	656	1280	22.806
	64	1564	3072	26.319
	128	3141	6152	31.453

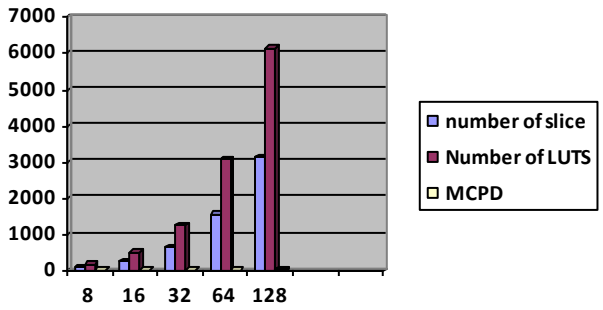

Fig. 12 Bar graph of the array multiplier

Table II. Result for complex number

Radix-2 DIT Algorithm for N=8 and N=16			
Parameter	**Number of Slice**	**Number of LUTs**	**MCPD (nsec)**
N=8	438	864	24.948
N=16	1168	2304	30.687

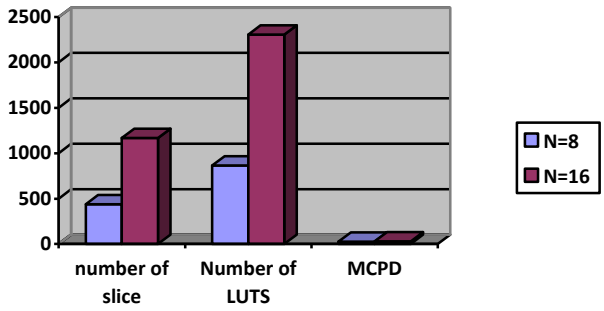

Fig. 13 Bar graph of the complex multiplier

4. CONCLUSION

The Fast Fourier transformation (FFT) is a frequently used Digital signal processing (DSP) algorithms for the applications of Orthogonal Frequency Division multiplexing (OFDM). The combination of Orthogonal Frequency Division Multiplexing (OFDM) with Multiple Input Multiple Output (MIMO) signal processing is a definite approach of enhancing the data rates of various communication systems such as Wireless LAN, e Mobile, 4G etc.

Since FFT processor is a complex module in OFDM, it is highly inevitable to design the processor in an efficient way. This research work involved the implementation of a low delay and area efficient 128-point pipelined FFT processor using radix-2 algorithm. The proposed algorithm is about 14- 15% consumed de in existing algorithm.

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